embedded world 2014 Exhibition&Conference
... it´s a smarter world

Arnold Wiemers

Special Construction Principles for Reliable High-speed PCBs

Revision 24.01.2014

in cooperation with

LeiterplattenAkademie ISW INDIVIDUALSOFTWARE ILFA Akademie

1 Introduction

Over the last years the development of electronic devices has changed significantly.
The simple reduction of geometrical structures has been replaced by increasing complexity and by linking different and demanding properties.

The design of future electronic devices cannot be managed with the previously used generalized strategies of CAD systems.

The competences required from designers have to be enhanced.

Introduction

There are some factors to be considered as requirements for an effective stack-up and a fail-safe function of a Highspeed-Device.

1st Power Integrity The standard decoupling of an electronic circuit can be provided broad-band through capacitive powerplanes with a layer distance of 50µm. Additionally only local capacitor groups have to be added.

2nd Signal Integrity Defined GND references for back current paths optimise signal integrity. If there are several signal layers it is useful to have several GND references.

3rd EMI EMI-emissions (internal + external) and/or the interference of a device is drastically reduced by plating the PCB edges.

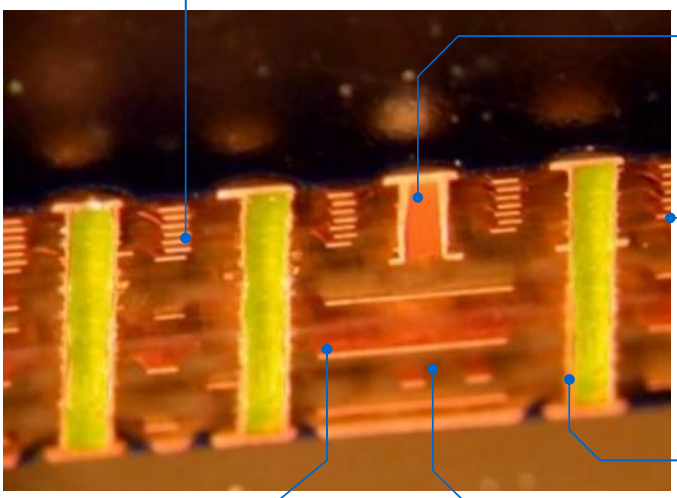
4th Self Interference Interferences on a device caused by its own VCC planes ("Internal EMI") is reduced to a minimum if the signal planes are shielded by GND planes against VCC.

Microsection of the PCB "Cero"

An MPS with layer distances of 50µm ensuring a capacitive power supply and optimizing the cooling

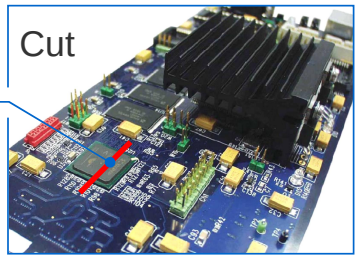
Term

MPS = **M**ulit**P**ower**S**ystem



Sequential BuriedVia

Cut



Plugged BGA vias

A stack-up minding EMI provides a high-grade signal integrity too

Parallel routed tracks allow the observance of a defined differential impedance

2 Base Material

Base material originally only had the task of being the mechanical carrier for the components. Still it serves as a platform for the wiring of the components.

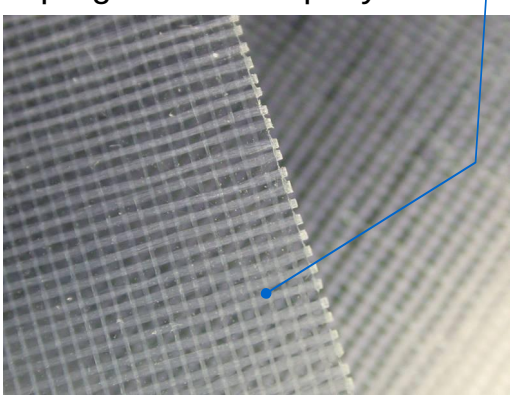
The technical and physical properties of base materials have increased in importance and influence. Even the construction of simple modules can no longer be done without the consideration of various material parameters.

For multilayer printed circuit boards and hybrids (e.g. Rigidflex PCBs) the material properties are often the decisive factor.

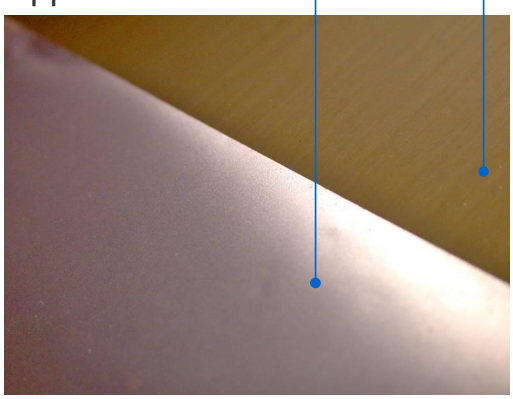
Base Material : Prepregs and Copper Foils

The base material for the construction of (FR4) base materials are copper foils and prepregs. In the laminates delivered by the base laminates manufacturer the epoxy resin is already completely cured. The prepregs are supplied separately and still have the ability to act as an adhesive under temperature and pressure. Pressed together the laminates and prepregs will form a solid composite. The roughened bottom of the copper foils increases the adhesion to the dielectric (e.g. prepreg).

Prepreg type 7628 (e.g. 180µm)
Glass fabric (warp and weft) impregnated with epoxy resin

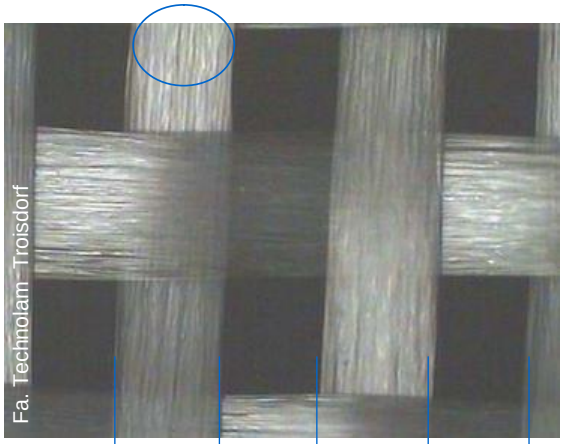


Copper foil 35µm
Lower side (roughened)
Upper side

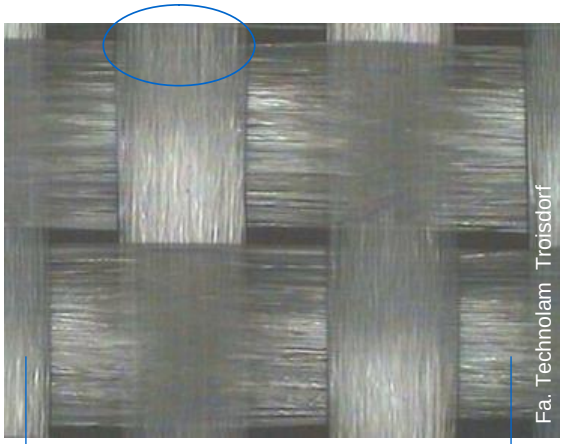


Impedance Deviance due to the Glass Fabric 1

Glass fabrics can have different structures. This effects the local continuity of the dielectric value. Both examples below show a prepreg type called "1080" even though the fibres are obviously different.



εr ~ 6.0 | εr ~ 3.8 | εr ~ 6.0 | εr ~ 3.8



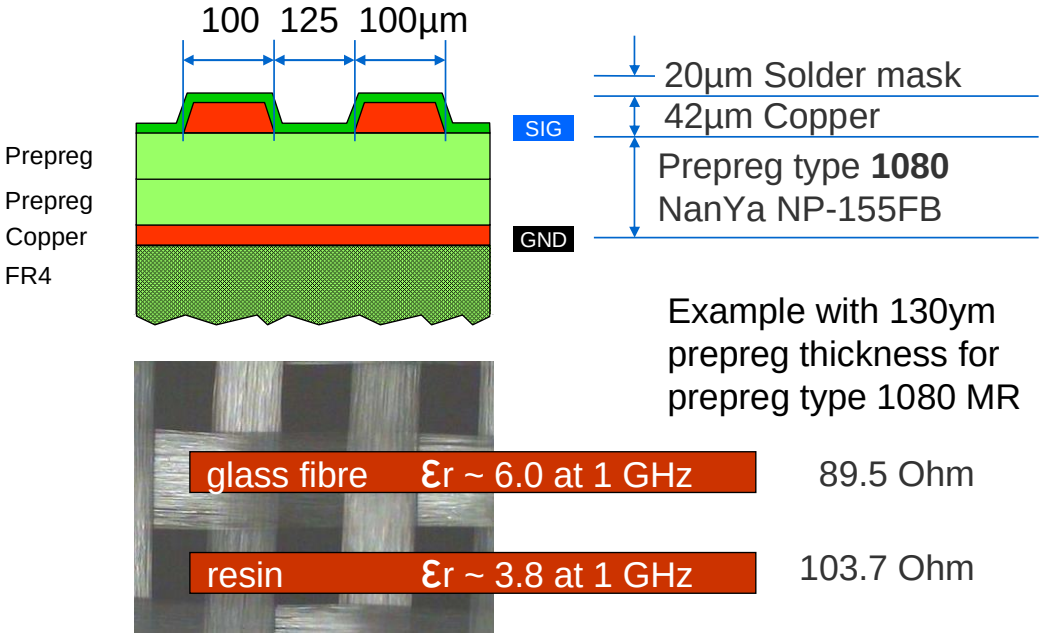
εr ~ 4.2

…. approximately at 1 GHz

Rule The propagation delay of a signal depends (...as well) on the location of the conductor on the prepreg surface.

Impedance Deviation due to the Glass Fabric 2

Impedance type "Differential Coated Microstrip"
(POLAR type "Edge-Coupled Coated Microstrip 1B")



The impedance values for conductors can show significant differences due to the dielectric environment caused by inhomogeneous glass fabric.

3 Drills and Plating Strategies

On a PCB different types of drill holes can be found.

Mounting holes are used for mounting component bodies, the adjustment of adjustable components and mounting the actual PCB in the housing of a device.

Component holes are used for mounting the THT components.

Vias (lasered or drilled) provide the electrical connection for signals travelling across different layers to connect the components of a PCB.
Therefore it is necessary to create electrical connections in Z-axis.

Drilling and metallization of THTs and/or vias provide the technical solutions for this demand.

Drills : Drill Classes within a Multilayer

In a multilayer various via types can be combined. As a result many strategies for power supply modules and for the wiring of the required signal traces are possible.

The layer stack-up must be coordinated to the desired via strategy. Therefore the layer stack-up must be defined before the layout job on the CAD system begins.

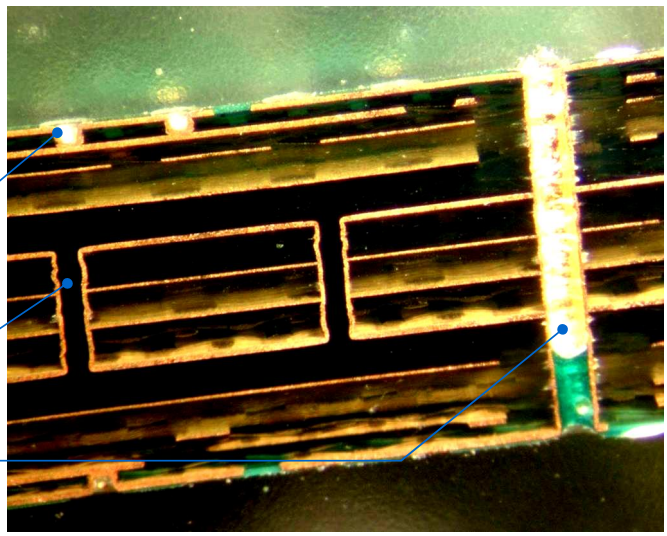
Example

Via types in a 12-layer board

BlindVia
(lasered)

BuriedVia
(drilled)

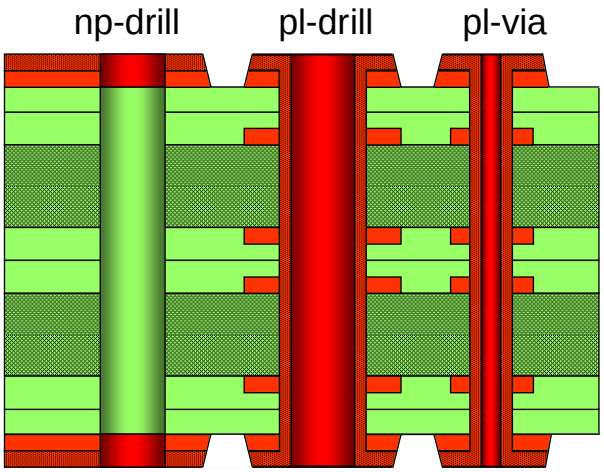
ThroughVia
(drilled)



Drills : Throughhole Vias

Definition (Throughhole via)

Mounting holes, component holes (~ THTs) and via holes (~ THT vias) cross *every* layer of a printed circuit board.



Table

Maximum contactable depth for plated through-holes at an AspectRatio of **1 : 8**.

Example

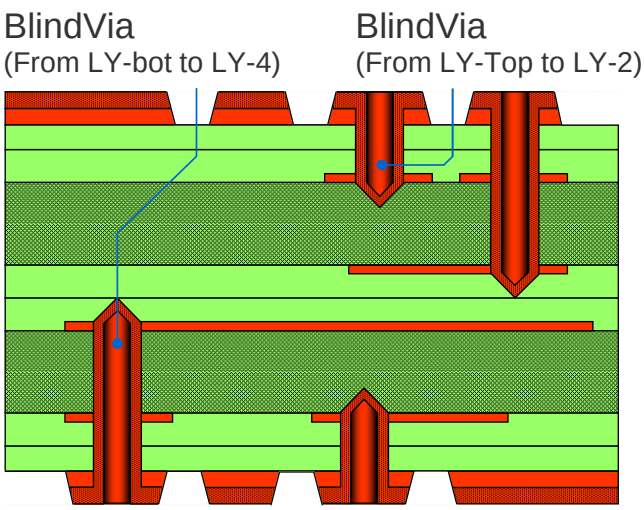
0.35 • **8** = **2.80** [mm]

CAD diameter	(mm)	0.05	0.10	0.15	0.20	0.25	0.30
Drill tool	(mm)	0.15	0.20	0.25	0.30	**0.35**	0.40
Drill depth	(mm)	1.20	1.60	2.00	2.40	**2.80**	3.20

Drills : BlindVias

Definition (BlindVias)

BlindVias connect one (…even temporary…) outer layer with *one or more* inner layers.



Table

Maximum contactable depth for BlindVias at an AspectRatio of **1 : 1**.

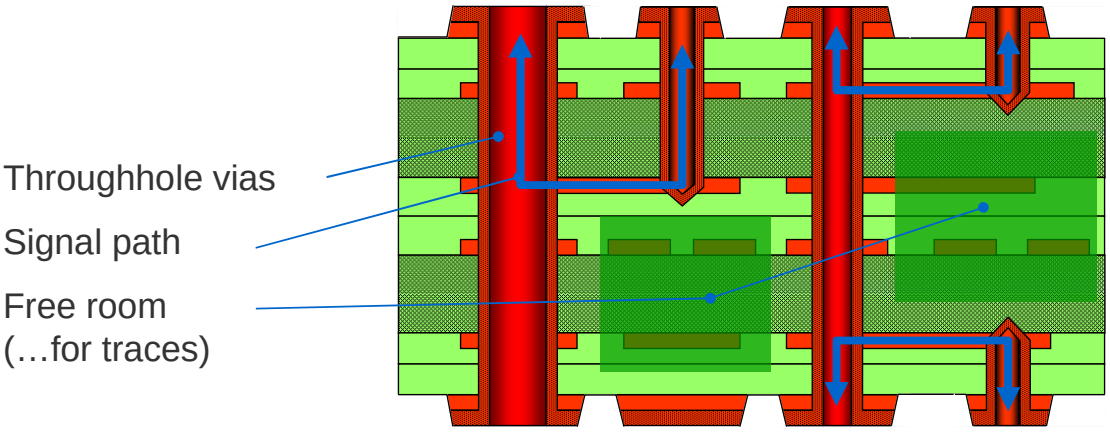
Example

0.30 • **1** = **0.30** [mm]

CAD diameter	(mm)	0.05	0.10	0.15	0.20	0.25	0.30
Drill tool	(mm)	0.15	0.20	0.25	**0.30**	0.35	0.40
Drill depth	(mm)	0.15	0.20	0.25	**0.30**	0.35	0.40

Drills : Via Strategies for Multilayer Boards 2

Vias in a 6-layer board : the signal connections are routed by using the THD component holes and the ThroughVias. As an additional option BlindVias enable short and effective signal traces from the top and the bottom layer.
The wiring is compact and creates rooms within the PCB to be used for the layout job.



Note

A direct pathway from net point to net point improves signal integrity and EMI behavior of an electronic device.

4 Edge Metallization

The metallization of the edges of a printed circuit board uses the third dimension of the PCB for a reliable technical function of the later device.

For instance steps to improve EMI behaviour can already be planned at the time of the PCB design.

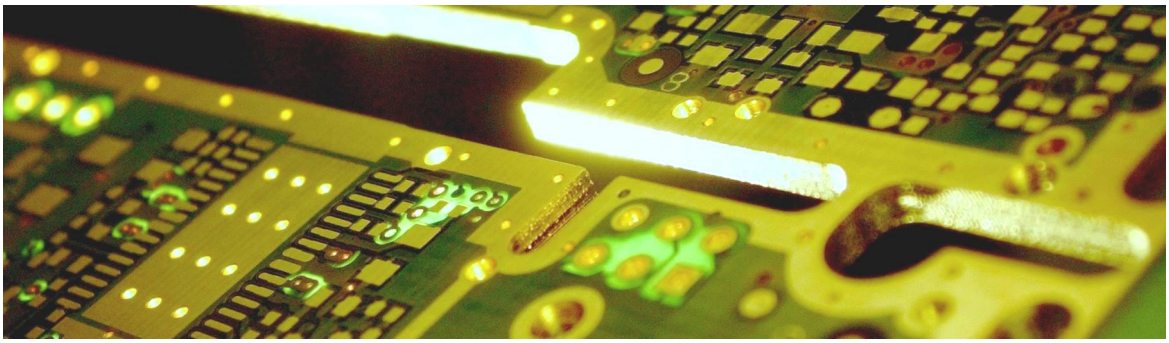
For the systematic work on a CAD layout there are aspects which lead to better results.
However, the demands for the documentation of a printed circuit board rise significantly.

Edge Metallization

Edge metallization means that copper is deposited at the edge of the printed circuit board first. Subsequently the final surface finish of the PCB is applied too.

The metallization of the edges is performed during the manufacturing step "plating". The contours of the metallized edges must have been milled *prior* to the plating of the PCB. In order to protect the copper from the later following etching process it must be covered with a metal resist.

The edge metallization surface is always flat. Sections of the circuit board as well as sections of contours of the PCB maybe partially metallized.



Edge Metallization : Options

The edge metallization enables technical and strategical tasks in very different areas.
The advantages of edge metallization arise particularly in multilayer boards (... from 6 layers on) if the GND planes are connected to the metallization.

Options

EMI	**E**lectro **M**agnetic **I**nterference : The interior region of a multilayer is shielded.
Cooling	The edge acts as an additional cooling area. The heat spreading is maximal. At the edge the heat can be actively dissipated.
PI	**P**ower **I**ntegrity : The properties of the power supply system are defined and controlled.
SI	**S**ignal **I**ntegrity : A reliable GND reference can be defined for signals travelling through connectors and cables.

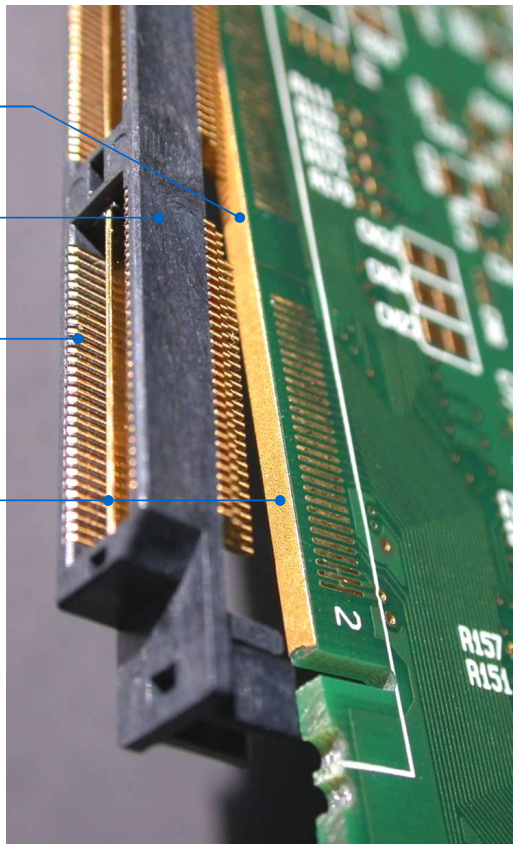
Surface Finish : Edge Metallization

In combination with the edge plating the surface finish may also be applied to metallize the edges of a PCB.

In conjunction with a suitable component (in this case a plug manufactured by Samtec) a high quality transfer of the signals from the circuit board to the periphery can be achieved (here : differential signal transmission).

A prerequisite is that the GND plane is connected to the edge metallization.

When the signal information passes the plug the reference potential is carried on the small plane in the middle of the connector which is in contact with the edge of the PCB.



5 Solder Resist + Silkscreen

Solder resist is used for preventing shorts during soldering, for isolating components against the PCB surface and for improving the electrical properties of the PCB.

Solder resist can be printed on all standard surfaces (tin, nickel, gold, silver and copper).

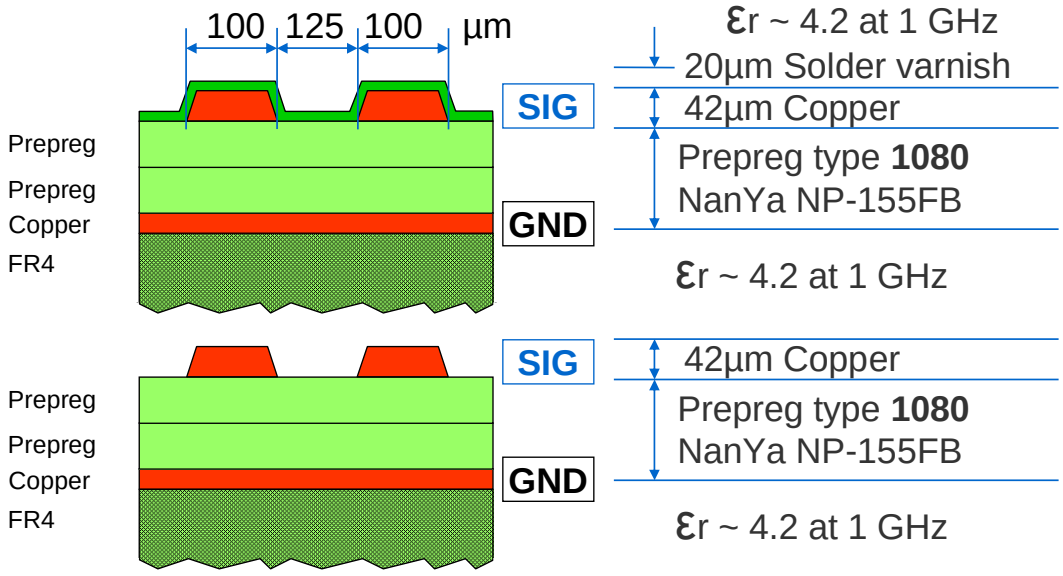
For impedance-defined PCBs the dielectric properties of the lacquer must be taken into consideration.

Silkscreen print is a 2-pack-epoxy resin, comparable to solder mask lacquer.

The print can be applied to all standard surfaces.

Impedance in Relation to Solder Resist

Impedance type "Differential Coated Microstrip"
(POLAR type "Edge-Coupled Coated Microstrip 1B")

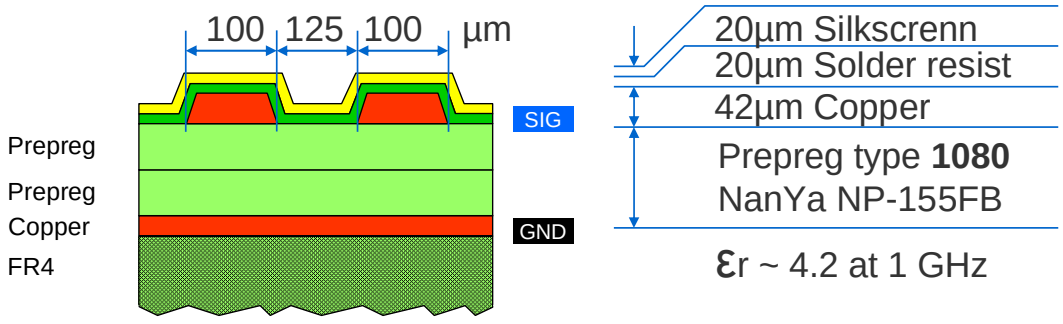


Impedance values with and without solder varnish			
MR - resin	71-8 = 63 • 2 = 126	99.9 Ohm	111.8 Ohm
MR + resin	71+8 = 79 • 2 = 158	104.4 Ohm	116.8 Ohm

Impedance Value in Relation to Silkscreen Print

Impedance type "Differential Coated Microstrip"
(POLAR type "Edge-Coupled Coated Microstrip 1B")

εr ~ 4.2 at 1 GHz for solder resist and for silkscreen



Impedance deviation with solder resist and with silkscreen			
MR - resin	71-8 = 63 • 2 = 126	99.9 Ohm	93.4 Ohm
MR + resin	71+8 = 79 • 2 = 158	104.4 Ohm	97.3 Ohm

6 Construction Classes

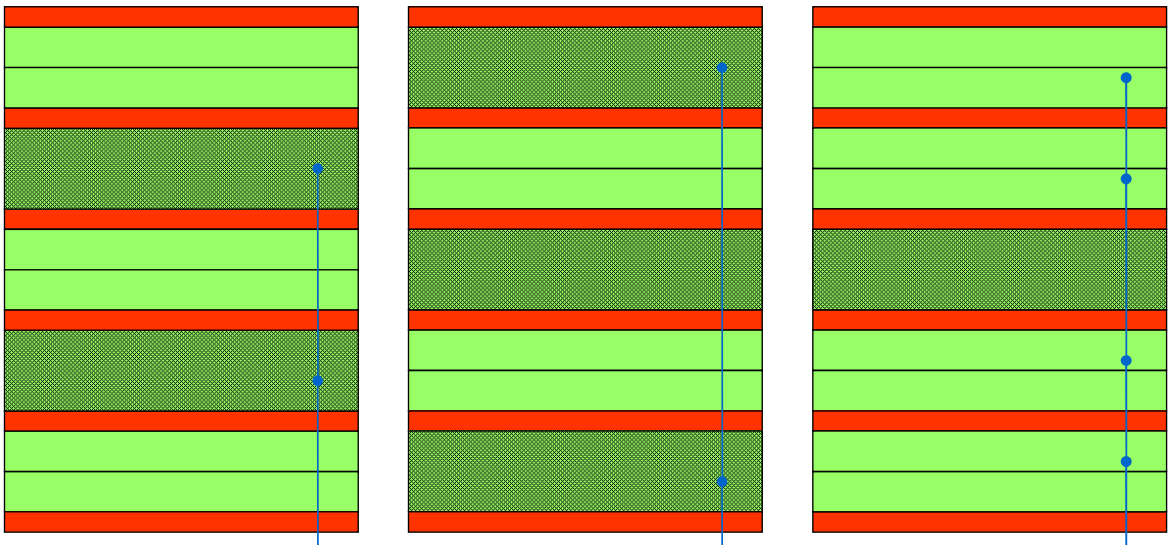
The combination of standard materials for multilayers (laminates, prepregs, copper foils) and the order of manufacturing and assembly steps result in different construction classes.

Each construction class has typical combinations of possible plating strategies.
Due to the alternating stack-up of prepregs and laminates in a multilayer there are typical construction variants.

Regarding function, CAD design and economic evaluation there are significant differences.

Multilayer Construction Classes

Laminates and prepregs can be arranged in different ways. But it is possible to define classes depending on the position of the cores in a multilayer. Due to these classes plating strategies and hybrid constructions for special tasks can be described.



Multilayer Construction with Cores Inside

Multilayer (...from 6 layers onwards) with inner cores are an *uncomplicated construction type*. This is a low-price version for highspeed assemblies.

Each laminate can be plated separately. Therefore a temporary double sided PCB or a 4-layer board can be produced.

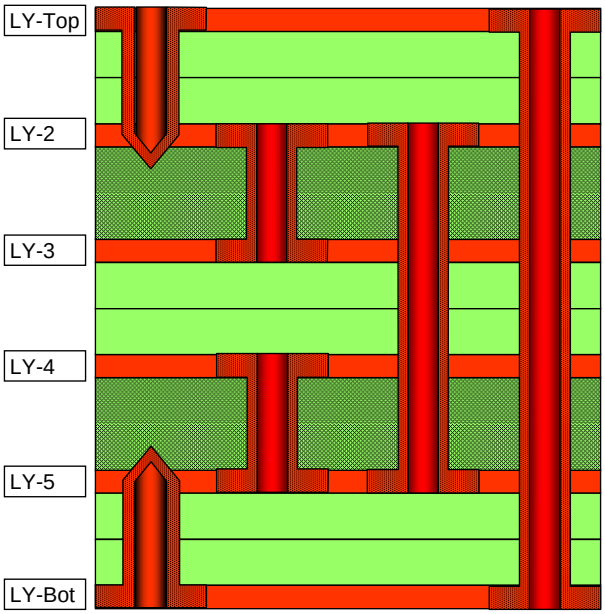
The outer layers can be connected by BlindVias.

For BGAs with a large number of pins to be connected an internal wiring is possible.

Large quantities are producable at acceptable costs.

Hybrids are not ideal.

6-Layer board with two inner cores.



Multilayer Construction with Cores Outside

Multilayer (...from 6 layers onwards) with cores outside are a good solution if *hybrids* shall be built.
This is a solution as well if a plating of outer cores is necessary due to the *AspectRatio*.

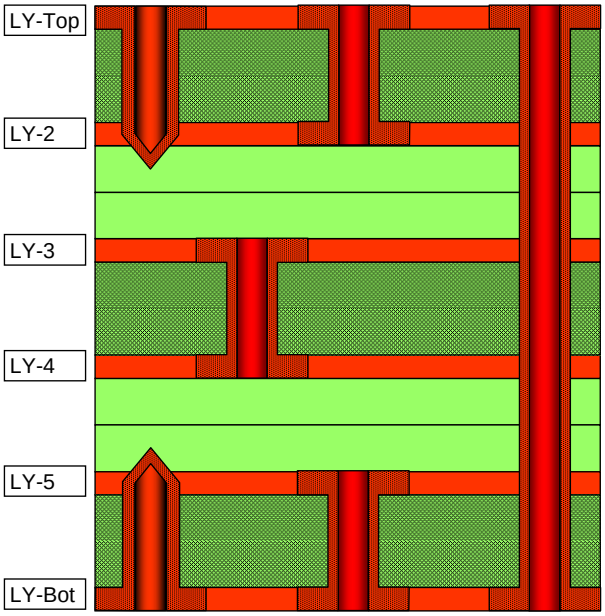
Uncomplicated highspeed assemblies are possible.

The inner core can be plated separately. The outer layers can be connected by BlindVias or by laser-vias without any problems.

For BGAs with a high pin count an internal wiring is possible.

Large quantities of PCBs are slightly more expensive.

6-Lagen board with two cores outside (...and one core necessarily inside).



Sequential Multilayer Construction

A multilayer with a sequential stack-up has no restrictions regarding to possible plating options.

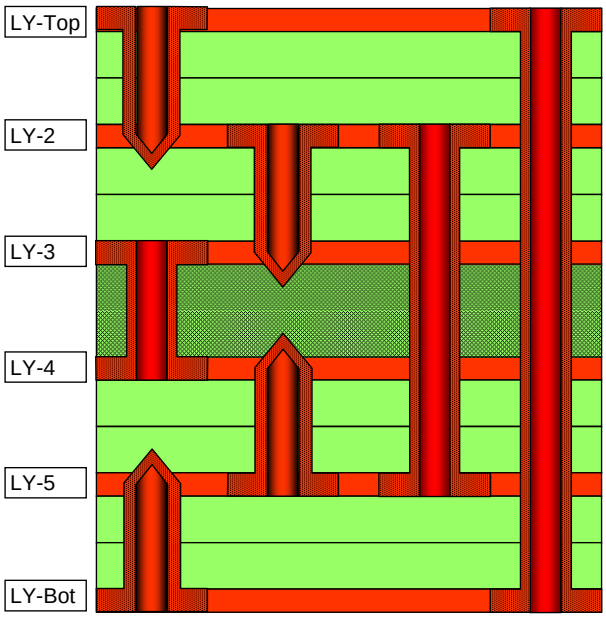
Highspeed assemblies are possible at low layer counts.

Sequential buildups need an additional pressing process. Due to material and production tolerances this buildup is not economical for small quantities of PCBs.

For connecting BGAs at a high pin count an internal wiring is possible.

Large quantities are expensive and often require via plugging.

6-Lagen board with one core in the middle and with prepreg attached layers on top and bottom.



7 Construction Rules

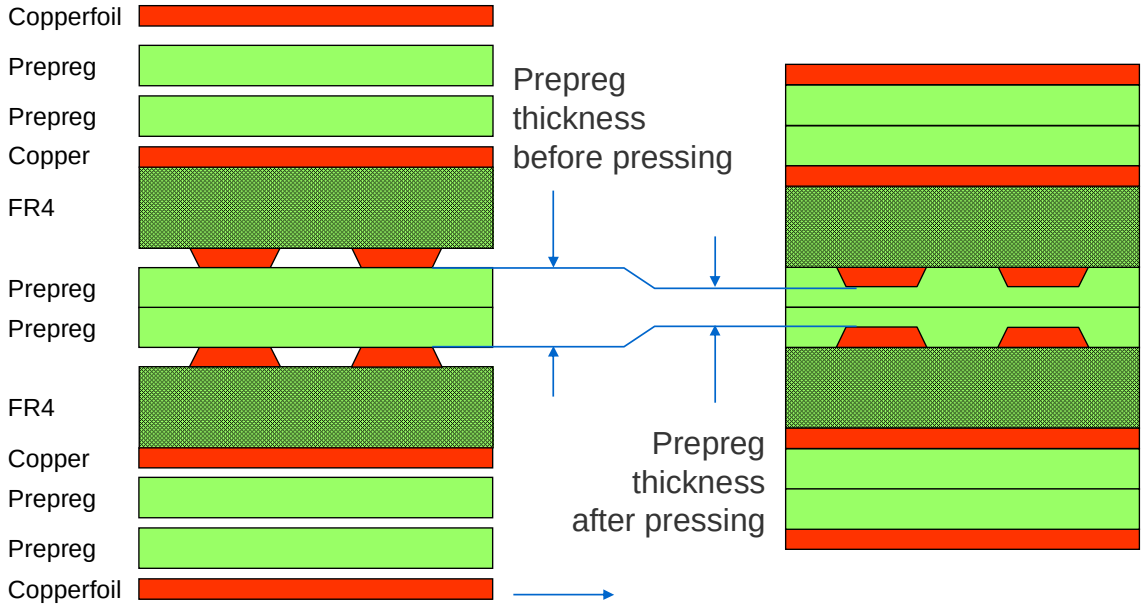
The pressing of a multilayer is a required manufacturing step if individual material components shall be reliably bonded together.
Functional requirements such as the impedance characteristics of a module depend on the reproducibility of the press technology.

Besides classical FR4 multilayer, rigid hybrid multilayer and rigidflex multilayer must be pressed with prepregs out of FR4 or different other materials.

The cooling of modules often requires the pressing of metal sheets like copper, bronze or aluminium.

Pressing : Influence on the Material Thickness

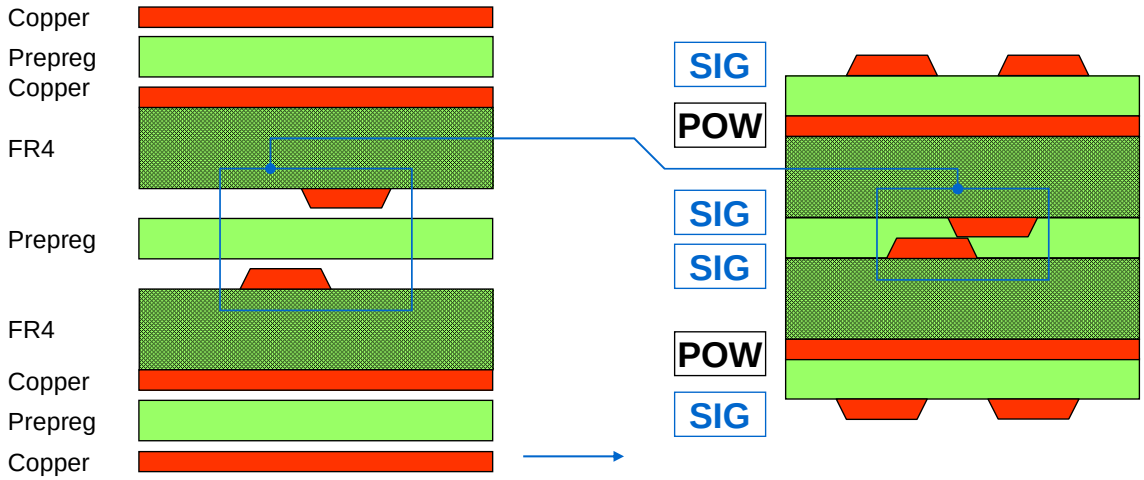
The epoxy resin of the laminates (~ cores) is cured, the resin of prepregs is not. Therefore the thickness of the laminates will not be influenced by the pressing process.



Rule During the pressing process the conductors are pressed into the epoxy resin of the prepregs.

Rule for inner Signal Layers

During pressing the complete multilayer the copper structures are pressed into the epoxy resin of the prepreg surface. This reduces the distance between electric structures on neighboured laminates, can cause short circuits and reduces the dielectric strength.

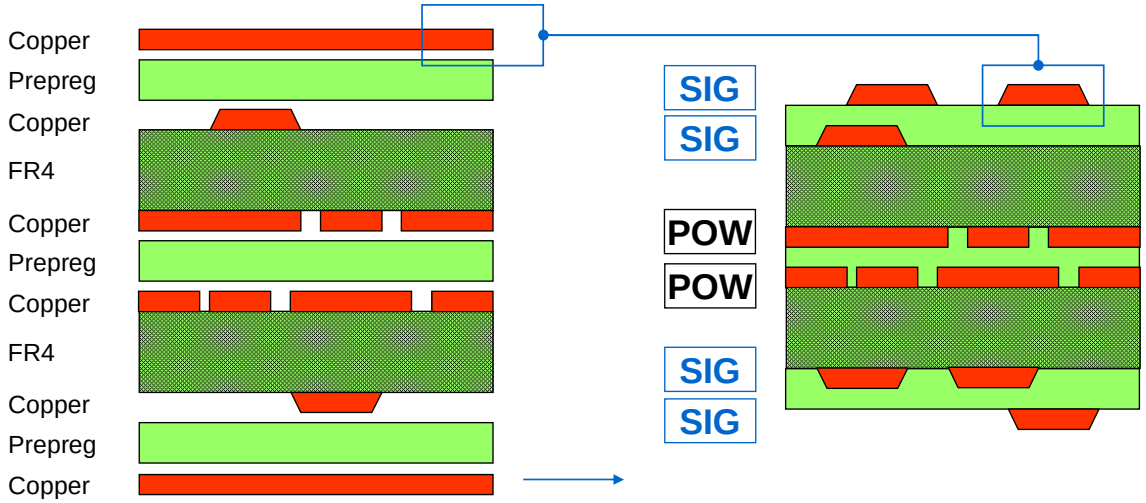


Rule The minimum prepreg thickness between two signal layers with a copper thickness of ≤ 17µm is 75µm.

Note It is recommended to insert *two* prepregs between signal layers.

Rule for Powerplanes and outer Signal Layers

Because the copper-powerplanes are flat they are pressed less into the prepreg surface than a signal layer. The outer layers are covered with copper foils which are structured *after* pressing the multilayer.



Rule The minimum prepreg thickness between two powerplanes with a copper thickness of ≤ 17µm is 50µm.

Note It is recommended to insert a prepreg with *medium* or *high resin* content.

General strategical Demands for Mounting

Rule (Adhesive option)

Adhesive substrates can *always* be bonded by adhesive and non-adhesive substrates.

Non-adhesive substrates *cannot* be connected to non-adhesive substrates.

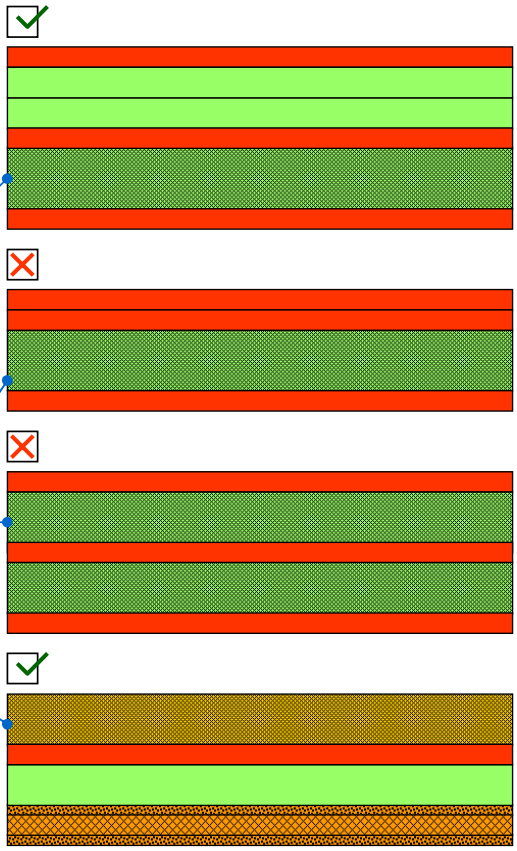
Example (Adhesive option)

CuFoil • Prepreg • Prepreg • Laminate
CuFoil • CuFoil • Laminate
Laminate • Laminate
Prepreg • Bond Ply • Laminate

Note (Adhesive option)

Adhesive substrates
Prepregs • Bond plys

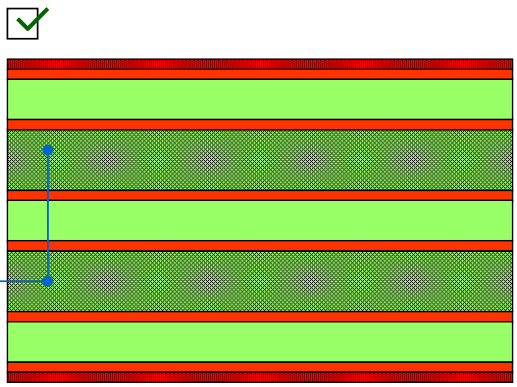
Non-adhesive substrates
Laminates • Metal sheets • CuFoils



General Construction Rules : Placement of Cores

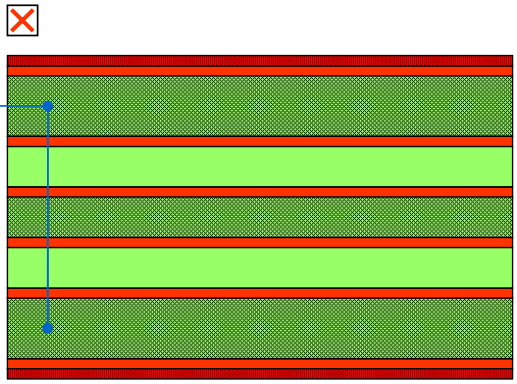
Rule (Cores inside/outside)

Multilayer boards for usual applications at a common thickness from 1.60 to 1.80mm should be constructed with stack-ups based on inner cores.



Inner cores

Outer cores



Rule (Symmetry of construction)

Multilayer boards up to 8 layers should be constructed symmetrically with reference to the centre line.

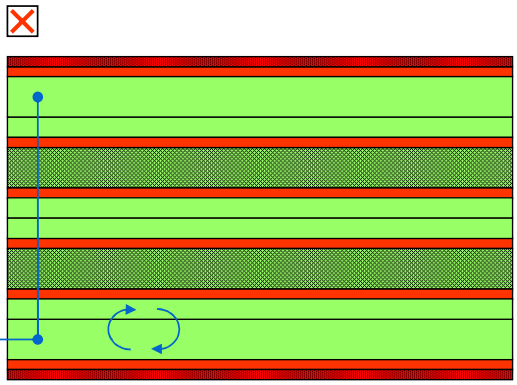
Note (Symmetry of construction)

Thereby bow and twist of the PCB should be avoided.

General Construction Rules : Order of Prepregs

Rule (Prepregs to outer layers)

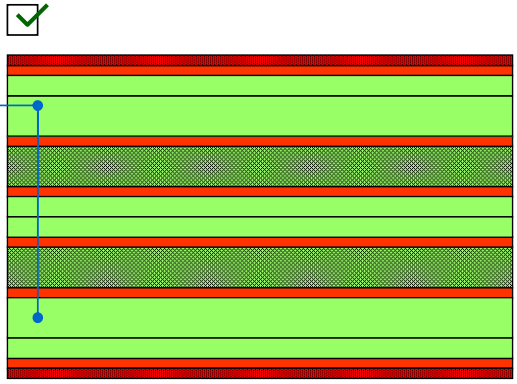
If the prepregs lying towards the outer layer of a multilayer have different thicknesses then the thinner prepreg should be placed nearer to the outer layer.



Prepregs outside

Note (Prepregs to outer layers)

Thinner prepregs have a thinner glass fabric. Therefore the prepreg surface has a planar structure.
This facilitates the pressing of the copper foil and the processing of the conductive pattern.
From a physical point of view the signal transmission quality increases.



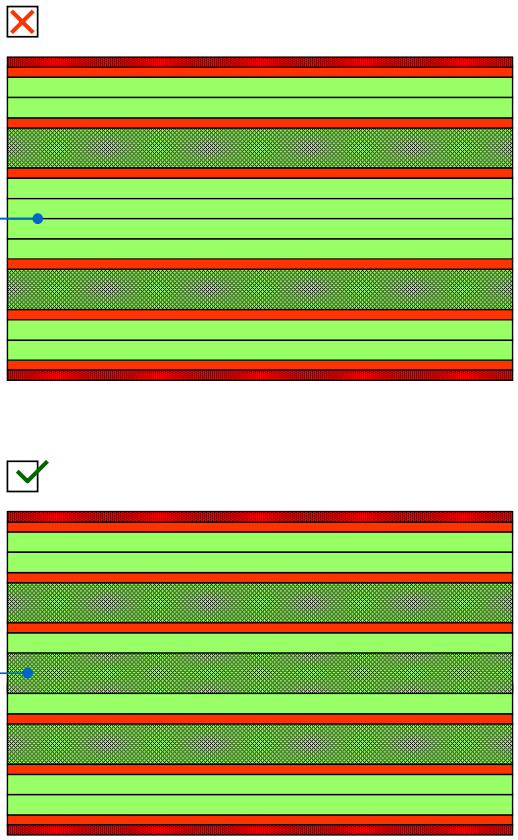
General Construction Rules : Maximal Number of Prepregs

Rule (Maximal number of prepregs)

More than 3 prepregs should not be mounted upon each other. Recommended are 2 prepregs.

Note (Maximal number of prepregs)

The materials for the stack-up will loose mechanical stability. This may result in cross warpage.



Rule (Filling inner sections of a multilayer)

If a filling of inner sections of a multi-layer board is only possible with more than 3 prepregs then an etched base laminate is to be used as a filling material.

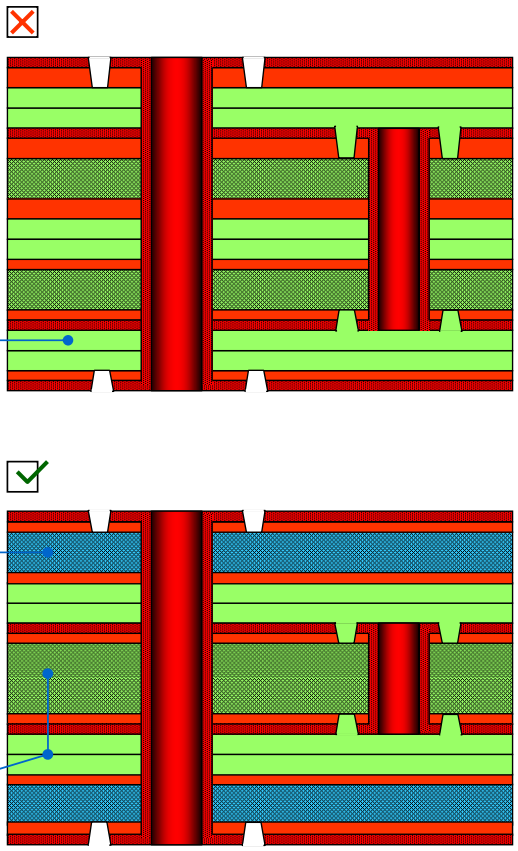
Special Construction Rules : Hybrid Construction

From a physical point of view FR4 is not the ideal material for many appli-cations
Because the signal transmission speed is coupled to the dielectric properties of the base material only "normal" data rates can be reached at an ε_r of 4.2.

Alternatively, laminates with low ε_r - values can be used, e.g. ceramic-filled substrates with an ε_r of 2.2.

Thus the physical benefits can only be used if these laminates are placed outside.

Because very often no prepregs of these special materials are available the complete stack-up of the multilayer has to be supplemented by conven-tional FR4 materials.



8 Multilayer Documentation

The need for the specification of layer stack-ups is not yet fully recognized.

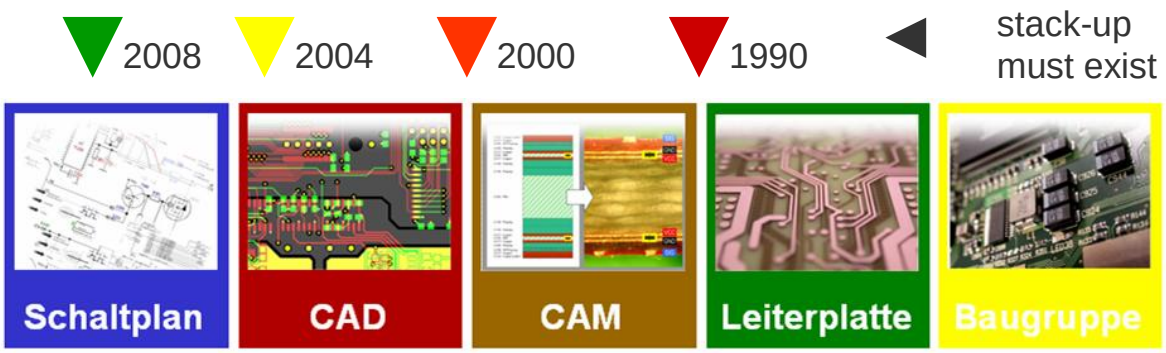
Layer stack-ups have to be defined already a long time before the CAD work begins.
Otherwise, how should it be possible to generate a meaningful analysis of the circuit function during working on the schematics ?

The right Time to present a Stack-up

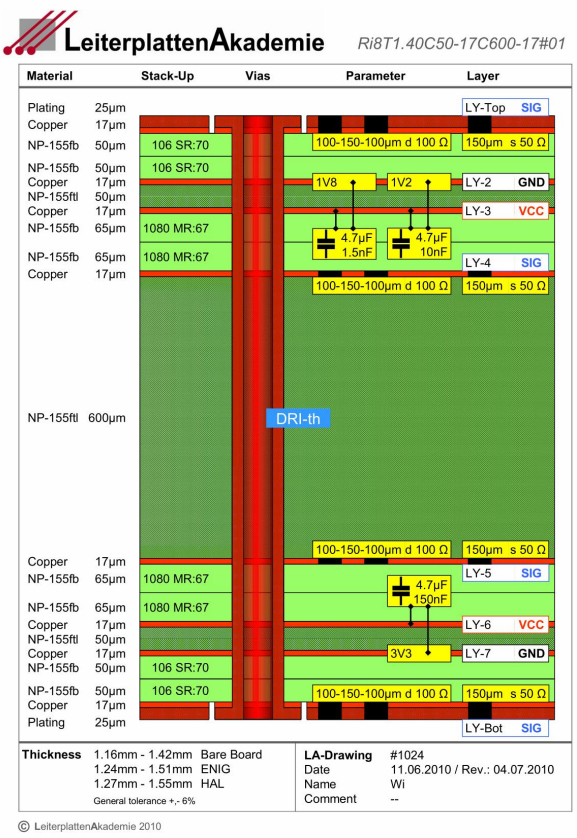
If an electronic device should be constructed five elementary tasks appear :

1 Generate the *concept* for the construction of the electronic unit
2 Generate the *circuit* and additional documents for CAD
3 Generate the *CAD Layout* and transfer production data to CAM
4 Produce *PCBs* and deliver to the assembly manufacturer
5 Produce *assemblies*, check function and deliver to the customer

A reliable multilayer stack-up must be defined before the circuit is finished. Otherwise it's not possible to plan and calculate essential properties (…like circuit simulation, function, processibility) of the subsequently assembled electronic device.



Documentation of Multilayer Boards



Particularly with regard to applications for highspeed devices the production of high-value multilayer boards should not be left to chance.

Material selection, layer stack-up, impedance class, impedance type and other physical demands on PCBs have to be reproducible documented.

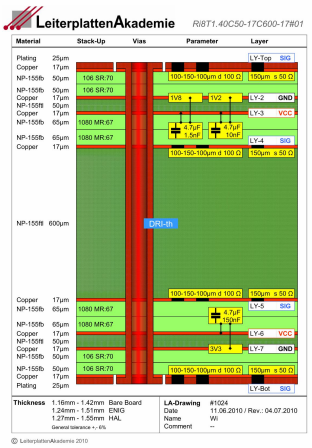
Rule (Multilayer documentation)

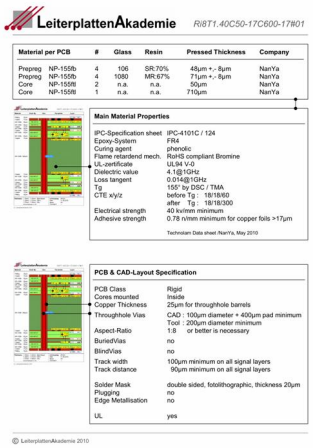
For ordering PCBs (…and even assembled devices) a multilayer documentation has to be a reliable specification which has a *technical* and even a *legal* quality.

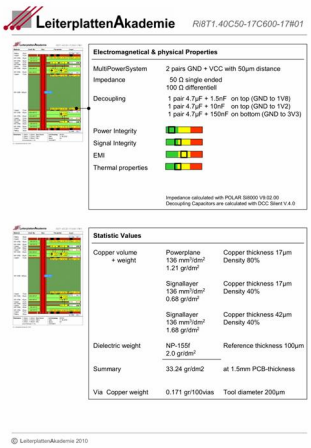
Documentation of Multilayer Stack-ups : Overview

The minimum documentation of a PCB must inform about :

- The *quality* and *quantity* of the material used
- The *technical parameters* of the base materials used
- The *PCB specification* including subqualities
- The *CAD constraints* including extreme values for the routing
- The *electro-physical characteristics* of the printed circuit board
- The main *volume parameters* for the production of assemblies







Standard documentation of a PCB by the *LeiterplattenAkademie*

9 Conclusion

Therefore ….. ?

Conclusion

The function of a multilayer or an assembly unit is not only defined by putting a number of base materials on a stack.

It has to be the strategy to integrate all partners from circuit design to PCB production and assembly.
This assumes **communication** on a high level.

Developed requirements must be integrated systematically.
Therefore a reliable **organisation** is needed.

Because assembly production is dynamically, **information** must be handled carefully.

A CAD Layout, a PCB or an assembly can only be done with a *reliability* directly proportional to the quality of information which is available during routing or producing or assembling the electronic device.

Materials and production processes must be known by all participants.

Professional responsibility decides. Only *qualified* and *continuous* education of all people who fabricate electronic devices guarantees a reliable function of highspeed units.

Thank You.

LeiterplattenAkademie

Contact

LA - LeiterplattenAkademie GmbH
Krefelder Straße 18
D-10555 Berlin

www.leiterplattenakademie.de

Managing Director
Kathrin Fechner

Telefon 030 / 34 35 18 99
Telefax 030 / 34 35 19 02

eMail
info@leiterplattenakademie.de

Technical Director
Arnold Wiemers

Telefon 0171 / 358 3712
Telefax 0531 / 126441

eMail
awi@leiterplattenakademie.de

Special construction principles for reliable Highspeed PCBs

embedded world 2014
Exhibition&Conference
... it´s a smarter world

Special Construction Principles for Reliable High-speed PCBs

Arnold Wiemers
LA - LeiterplattenAkademie GmbH
10555 Berlin, Germany

Abstract **- The CAD-Layout of reliable high-speed applications must consider elementary rules for manufacturing printed circuit boards. The modular construction of multilayer stack-ups supports functional and reproducable multilayer systems.**

Keywords – multilayersystems; base material; High-speed PCBs; impedance; edge metallization; plating; solder mask; silkscreen; signal integrity; stack-up technologies;

I. INTRODUCTION

The printed circuit board mediates between the construction and the CAD layout on one side and between the production of the assembly on the other. With increasing signal rise times and a growing volume of information to be processed, the physical requirements for printed circuit boards have increased. The comprehensive knowledge of rules for the production and function of an electronic device will be an essential prerequisite for the construction of a reliable assembly. Meanwhile electro-physical requirements have to be added, such as signal integrity and power integrity. Not at least the predictable quality of an assembly to be constructed is more and more important.

Over the last years the development of electronic devices has changed significantly. The simple reduction of geometrical structures has been replaced by increasing complexity and by linking different and demanding properties. The design of future electronic devices cannot be managed with the previously used generalized strategies of CAD systems. The competences required from designers have to be enhanced.

There are some factors to be considered as requirements for an effective stack-up and a fail-safe function of a Highspeed-Device (Fig. 1.).

Power Integrity : The standard decoupling of an electronic circuit can be provided broad-band through capacitive powerplanes with a layer distance of 50µm. Additionally only local capacitor groups have to be added.

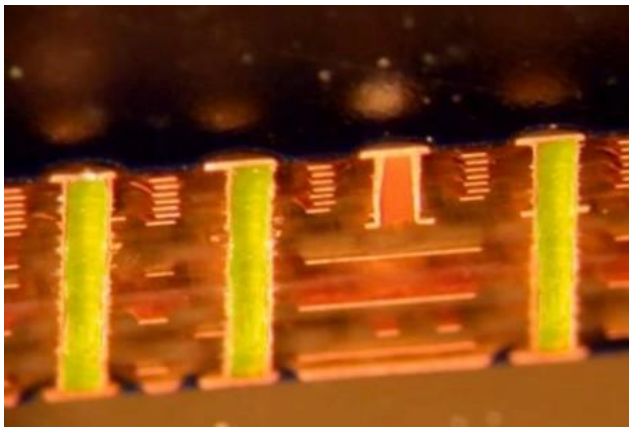
Signal Integrity : Defined GND references for back current paths optimise signal integrity. If there are several signal layers it is useful to have several GND references.

EMI : EMI-emissions and interference of a device are reduced by plating the PCB edges.

Self Interference : Interferences on a device caused by its own VCC planes ("Internal EMI") is reduced if the signal planes are shielded by GND planes against VCC.

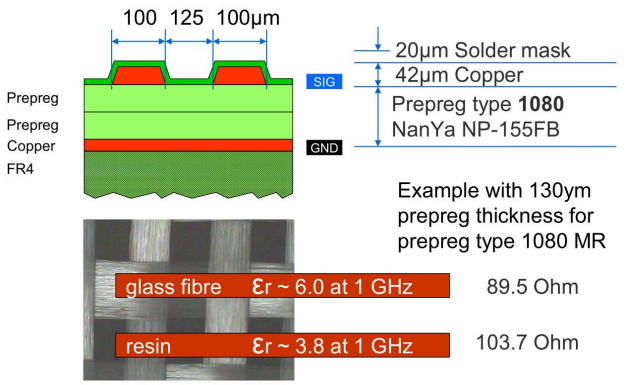
II. BASE MATERIALS

Base material originally only had the task of being the mechanical carrier for the components. Still it serves as a platform for the wiring of the components. The technical and physical properties of base materials have increased in importance and influence. Even the construction of simple modules can no longer be done without the consideration of various material parameters (Fig. 2.).



Throughhole vias are plugged with epoxy resin. Multipowersystem in the above section with a sequential BlindVia. Differential transmission lines between GND-planes in the middle section below .

Fig. 1. Cross section of an 18-layer-board.



Reliable differential signaling depends on data transmission without delay between the tracks. FR4 material with too large spacing between the glas fibres causes an uncontrolled and unequal transmission speed.

Fig. 2. Tracks for differential data transmission

For multilayer printed circuit boards and hybrids (e.g. Rigidflex PCBs) the material properties are often the decisive factor. The base material for the construction of FR4 base materials are copper foils and prepregs. In the laminates delivered by the base laminates manufacturer the epoxy resin is already completely cured. The prepregs are supplied separately and still have the ability to act as an adhesive under temperature and pressure. Pressed together the laminates and prepregs will form a solid composite. The roughened bottom of the copper foils increases the adhesion to the dielectric (e.g. prepreg).

Prepregs consists of glass fabric coated with epoxy resin. In addition to the prepregs there are only copper foils used to built PCBs. These are the basic materials for every electronic device. If a laminate (i.e. core) shall be produced several prepregs and copper foils on one or both sides are mounted and glued together.

III. Drilling Strategies

On a PCB different types of drill holes can be found. Mounting holes are used for mounting component bodies, the adjustment of adjustable components and mounting the actual PCB in the housing of a device. Component holes are used for mounting the THT components. Vias (lasered or drilled) provide the electrical connection for signals travelling across different layers to connect the components of a PCB. Therefore it is necessary to create electrical connections in Z-axis. Drilling and metallization of THTs and/or vias provide the technical solutions for this demand.

Holes in multilayer boards are essential. Depending on the increasing complexity the holes must be grouped into "holes for the reception of THT components" and "via holes".

Vias can be processed as throughholes (e.g. THV or Through Hole Via), or as a partial via (e.g. BlindVia, BuriedVia). BlindVias (Fig. 3.) can be produced either with laser technology (i.e. ablation) or with conventional drilling machines (i.e. cutting). The increasing density of wiring on a given PCB area necessarily leads to reduced via diameters. This influences the ability of plating the via barrels by using available galvanic processes.

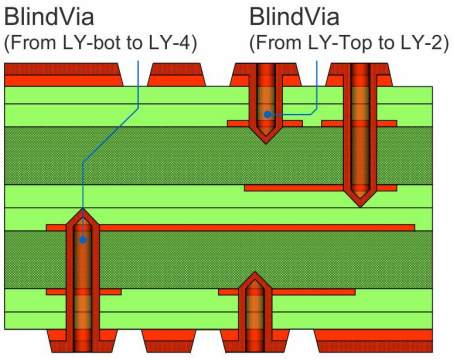
For the construction of highspeed multilayers these context must be considered. In a multilayer various via types can be combined. As a result many strategies for power supply modules and for the wiring of the required signal traces are possible. The layer stack-up must be coordinated to the desired via strategy. Therefore the layer stack-up must be defined before the layout job on the CAD system begins.

When working on a CAD design several parameters must be declared in advance. The possible routing geometries of traces and the integration of vias into a signal path must be known by the designer. The "AspectRatio (...for drills)" is a very important reference value to be considered if padstacks are generated on the CAD system.

Definition (AspectRatio for Drills)

The AspectRatio describes the mathematical relationship between the minimum hole diameter and the depth of the drill which can reliably be plated by a galvanic process.

Vias are placed on the CAD system to generate the fan-out for the signals, to route the signal connections and to connect the electronic devices to the power supply. Very often a connection is routed only on two layers. Every via hole used for this connection takes space on the other not used layers. This lost space cannot be used for other tracks. Therefore, if necessary, additional signal layers must be inserted to complete the routing.



If BlindVias are routed the via geometry must be calculated due to the AspectRatio.
Otherwise the copper plating of via holes can be problematic during PCB production.

Fig. 3. Multilayer stack-up with BlindVias

IV. EDGE METALLIZATION

The metallization of the edges of a printed circuit board uses the third dimension of the PCB for a reliable technical function of the later device. For instance steps to improve EMI behaviour can already be planned at the time of the PCB design. For the systematic work on a CAD layout there are aspects which lead to better results. However, the demands for the documentation of a printed circuit board rise significantly.

Edge metallization means that copper is deposited at the edge of the printed circuit board first. Subsequently the final surface finish of the PCB is applied too. The metallization of the edges is performed during the manufacturing step "plating". The contours of the metallized edges must have been milled prior to the plating of the PCB. In order to protect the copper from the later following etching process it must be covered with a metal resist.

The edge metallization surface is always flat. Sections of the circuit board as well as sections of contours of the PCB maybe partially metallized (Fig. 4).

The edge metallization enables technical and strategical tasks in very different areas. The advantages of edge metallization arise particularly in multilayer boards (... from 6 layers on) if the GND planes are connected to the metallization.

Options

Electro **M**agnetic **I**nterference : The interior region of a multilayer is shielded.

Cooling : The edge acts as an additional cooling area. The heat spreading is maximal. At the edge the heat can be actively dissipated.

Power **I**ntegrity : The properties of the power supply system are defined and controlled.

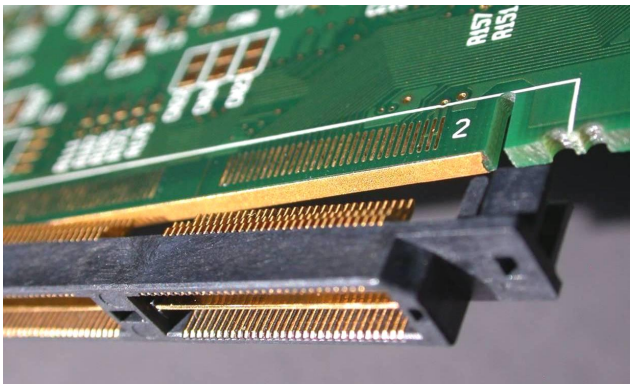
Signal **I**ntegrity : A reliable GND reference can be defined for signals travelling through connectors and cables.

The edge metallization of printed circuit boards allows extensive shielding of the interior region of the PCB with regard to EMI. The parts of the contour must be milled before plating. For further following process steps the individual PCBs are held in the production panel by webs. The edge area additionally serves for heat dissipation.

V. SOLDER RESIST + SILKSCREEN

Solder resist is used for preventing shorts during soldering, for isolating components against the PCB surface and for improving the electrical properties of the PCB. Solder resist can be printed on all standard surfaces (tin, nickel, gold, silver and copper).

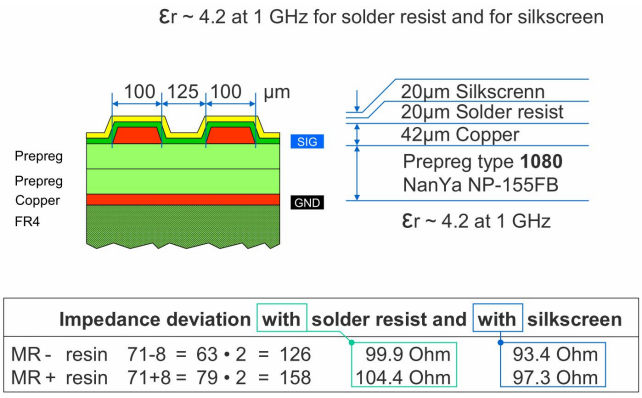
Solder resist lacquers are thermally-hardening 2-pack-epoxy lacquers which are mainly structured in photo technical procedures. For impedance-defined PCBs the dielectric properties of the lacquer must be taken into consideration (Fig. 5).



The edge of the PCB is partially plated and covered with a surface finish (...ENIG in this case). As a result the internal GND-plane of the PCB contacts a small plane in the middle of the plug. Thus the differential signals on top and bottom of the PCB still have a reference to GND when passing the connector.

Fig. 4. Multilayer with edge metallization and highspeed connector

The coating with solder resist may be structured by screen printing on the PCB. For printed circuit boards belonging to the class "HDI" or for SMD circuit boards generally a coating with a photo sensitive liquid film is preferred that can be laminated, rolled or sprayed on. The structuring of the solder resist is done by film or (…seldom) by laser. The registration of the film for processing the solder resist takes place with low tolerance and high accuracy directly before exposure.



Solder resist and silkscreen are based on epoxy resin. The used substrates have a dielectric value which must be taken into account when calculating impedance values.

Fig. 5. The influence of lacquers on impedance values

The position of components can be marked on PCBs by silkscreen. Information can be provided for device production, the operation or the service of the PCB (blocked areas, information about operating voltage or warnings about high voltage and the like). Silkscreen print is a 2-pack-epoxy resin, comparable to solder mask lacquer. The print can be applied to all standard surfaces.

Screen printing methods are usually used to apply the silkscreen. The task of silkscreen print is to identify the position of components on the printed circuit board, to mark the polarity of components and to identify the position of jumpers.

The dielectric properties of the silkscreen varnish are comparable with the dielectric properties of the solder lacquer. Silkscreen covering conductors has an influence on the impedance and thus changes the signal propagation delay.

VI. Construction Classes

The construction of a multilayer system orientates on the functional demands, the production technology and the economic conditions.

Usually it's not possible to fulfil all demands. The task is to find an individual solution fulfilling most of the demands for a projected device. Selection and sequence of laminates determine plating strategy and therefore the constraints needed on a CAD system. Even on larger PCB series the costs are determined by the volumes of prepregs and laminates as well as the drilling technology meaning the efficiency of connecting strategies and technologies.

The complex construction of multilayer systems allow solutions for electronic products on a high end level. The need for the specification of layer stack-ups is not yet fully recognized. Layer stack-ups have to be defined already a long time before the CAD work begins.

If an electronic device should be constructed, five elementary tasks appear :

1. Generate the concept for the construction of the electronic unit
2. Generate the circuit and additional documents for CAD
3. Generate the CAD Layout and transfer production data to CAM
4. Produce PCBs and deliver to the assembly manufacturer
5. Produce assemblies, check function and deliver to the customer

A reliable multilayer stack-up must be defined *before* the circuit is finished. Otherwise it's not possible to plan and calculate essential properties (…like circuit simulation, function, processibility) of the subsequently assembled electronic device.

There are some factors to be considered as requirements for an effective stack-up and a fail-safe function of a Highspeed-Device :

Power Integrity

The standard decoupling of an electronic circuit can be provided broad-band through capacitive power-planes with a layer distance of 50µm. Additionally only local capacitor groups have to be added.

Signal Integrity

Defined GND references for back current paths optimise signal integrity. If there are several signal layers it is useful to have several GND references.

EMI

EMI-emissions (internal + external) and/or the interference of a device is drastically reduced by plating the PCB edges.

Self Interference

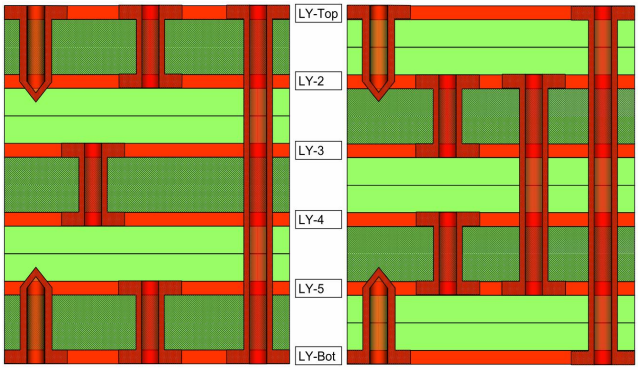
Interferences on a device caused by its own VCC planes ("Internal EMI") is reduced to a minimum if the signal planes are shielded by GND planes against VCC.

Developers face an ever increasing demand regarding pace and complexity in development of electronic devices driven by both technological and economical requirements. These requirements cannot be met anymore by the strategies of the past years (e.g. simple reduction of geometrical structures).

Today's CAD-Systems still not provide sufficient support in managing all the requirements arising from electronic and physical properties, function, manufacturing, assembly and test.

Only profound knowledge of the designer in all these related fields will lead to success.

The pressing of a multilayer is a required manufacturing step if individual material components shall be reliably bonded together. Functional requirements such as the impedance characteristics of a module depend on the reproducibility of the press technology.



Multilayer stack-ups for a common 6-layer-board with cores outside (left side) or cores inside (left side).

Fig. 6. Stack-up strategies for rigid mulitlayer boards

Besides classical FR4 multilayer boards, rigid hybrid multilayer and rigidflex multilayer must be pressed with prepregs out of FR4 or different other materials. The cooling of modules often requires the pressing of metal sheets like copper, bronze or aluminium.

The construction of a multilayer system orientates on the functional demands, the production technology and the economic conditions.

Rule (Adhesive option) :

Adhesive substrates can always be bonded by adhesive and non-adhesive substrates. Non-adhesive substrates cannot be connected to non-adhesive substrates.

The combination of standard materials for multilayers (laminates, prepregs, copper foils) and the order of manufacturing and assembly steps result in different construction classes. Each construction class has typical combinations of possible plating strategies. Due to the alternating stack-up of prepregs and laminates in a multilayer there are typical construction variants.

Regarding function, CAD design and economic evaluation there are significant differences. Laminates and prepregs can be arranged in different ways. But it is possible to define classes depending on the position of the cores in a multilayer. Due to these classes plating strategies and hybrid constructions for special tasks can be described.

Cores Inside :

Multilayer (...from 6 layers on-wards) with inner cores are an uncomplicated construction type. This is a low-price version for highspeed assemblies.

Each laminate can be plated separately. Therefore a temporary double sided PCB or a 4-layer board can be produced. The outer layers can be connec-ted by BlindVias. For BGAs with a large number of pins to be connected an internal wiring is possible. Large quantities are producable at acceptable costs. Hybrids are not ideal (Fig. 6).

Cores Outside :

Multilayer (...from 6 layers on-wards) with cores outside are a good solution if hybrids shall be built. This is a solution as well if a plating of outer cores is necessary due to the AspectRatio.

Uncomplicated highspeed assemblies are possible. The inner core can be plated separately. The outer layers can be connected by BlindVias or by lasered vias without any problems. For BGAs with a high pin count an internal wiring is possible. Large quantities of PCBs are slightly more expensive (Fig. 6).

Sequential Multilayer Construction :

Multilayer (...from 6 layers onwards) with cores outside are a good solution if hybrids shall be built.

This is a solution as well if a plating of outer cores is necessary due to the AspectRatio. Uncomplicated highspeed assemblies are possible. The inner core can be plated separately. The outer layers can be connected by BlindVias or by lasered vias without any problems. For BGAs with a high pin count an internal wiring is possible. Large quantities of PCBs are slightly more expensive.

VII. Construction Rules

There are a number of elementary rules which must be considered when multilayer stack-ups are generated. For instance multilayer boards for usual applications at a common thickness from 1.60 to 1.80mm should be constructed with stack-ups based on inner cores. Keep in mind the following rules.

Multilayer boards up to 8 layers should be constructed symmetrically with reference to the centre line.

If the prepregs lying towards the outer layer of a multilayer have different thicknesses then the thinner prepreg should be placed nearer to the outer layer.

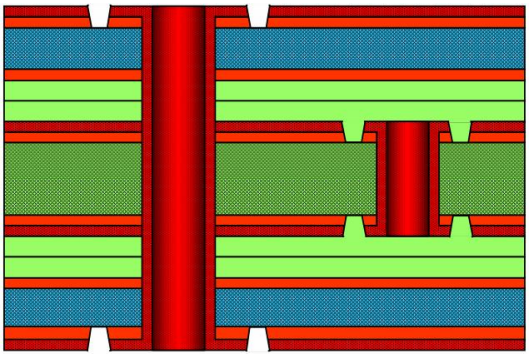
More than 3 prepregs should not be mounted upon each other. Recommended are 2 prepregs.

If a filling of inner sections of a multilayer board is only possible with more than 3 prepregs then an etched base laminate is to be used as a filling material.

The copper thickness on start and target layer of a plated via should be equal.

The copper thickness on both sides of a laminate should be equal.

From a physical point of view FR4 is not the ideal material for many applications



Because very often no prepregs of special materials are available the complete stack-up of the multilayer has to be supplemented by conventional FR4 materials and the special material cores have to move to the outside.

Fig. 7. A hybrid multilayer stack-up with special material cores outside

Because the signal transmission speed is coupled to the dielectric properties of the base material only "normal" data rates can be reached at an εr of 4.2. Alternatively, laminates with low εr -values can be used, e.g. ceramic-filled substrates with an εr of 2.2. Thus the physical benefits can only be used if these laminates are placed outside (Fig. 7.).

Because very often no prepregs of these special materials are available, the complete stack-up of the multilayer has to be supplemented by conventional FR4 materials.

VIII. Documentation Of Multilayer Boards

The need for the specification of layer stack-ups is not yet fully recognized. Layer stack-ups have to be defined already a long time *before* the CAD work begins. Otherwise, how should it be possible to generate a meaningful analysis of the circuit function during working on the schematics ?

If an electronic device should be constructed a number of elementary tasks appear :

- Generate the concept for the construction of the electronic unit
- Generate the circuit and additional documents for CAD
- Generate the CAD Layout and transfer production data to CAM
- Produce PCBs and deliver to the assembly manufacturer
- Produce assemblies, check function and deliver them to the customer

A reliable multilayer stack-up must be defined before the circuit is finished. Otherwise it's not possible to plan and calculate essential properties (…like circuit simulation, function, processibility) of the subsequently assembled electronic device. Particularly with regard to applications for highspeed devices the production of high-valuable multilayer boards should not be left to chance.

Material selection, layer stack-up, impedance class, impedance type and other physical demands on PCBs have to be reproducible documented. For ordering PCBs (…and even assembled devices) a multilayer documentation has to be a reliable specification which has a technical and even a legal quality.

The minimum documentation of a PCB must inform about :

- The quality and quantity of the material used
- The technical parameters of the base materials used
- The PCB specification including subqualities
- The CAD constraints including extreme values for the routing
- The electro-physical characteristics of the printed circuit board
- The main volume parameters for the production of assemblies

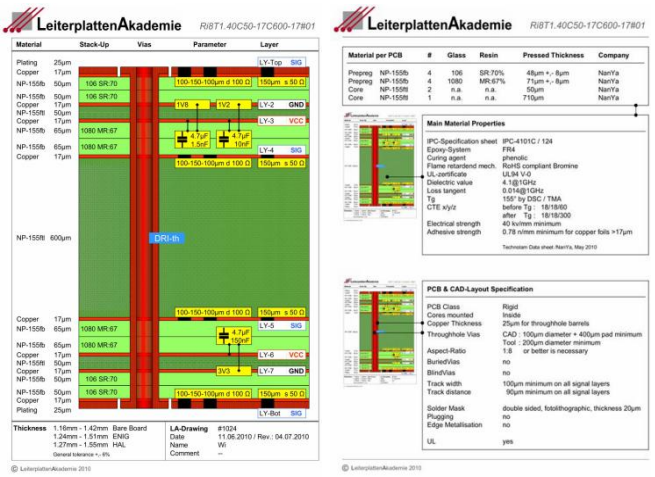
The classic description of a multilayer is not enough any more. The material properties need to be described in detail. The precise nomenclature of the materials is essential. The technical properties of base materials have to be listed free of doubt in the according documentation of a multilayer stack-up.

A reference to standard guidelines like DIN EN or IPC is necessary. The declaration of elementary physical properties is necessary.

Today every multilayer is associated with a designated application. The technical characteristics of an individual PCB not only have to be described by the documentation of the requirements for the quality of the printed circuit board but in either case must also be traceable disclosed and comprehensible. The repeatability of the production of a printed circuit board (...+ device) in case of a layout revision is only ensured with a meaningful documentation.

The PCB specification not yet defines the dedicated features of the product "assembly device". Therefore, prior to the assembly and circuit development, for the technologist the properties of a multilayer are not provided with the required transparency. A secure decision is possible if the physical properties of a stack-up can be reliably predicted (Fig. 8.).

The production of the assembly is usually not included in the preview when constructing a multilayer stack-up. Regarding the preliminary planning of systematic and reliable soldering profiles (for which surface ...?) this is a fatal deficiency. However, the problem is that there is no spectrum of requirements. The parameters required for an assembly production must be developed yet.



The documentation of a multilayer stack-up must provide CAD, PCB-manufacturing and assembly with detailed information about material properties and technical parameters bevor a project gets started.

Fig. 8. Documenation of a multilayer stack-up with necessary information

IX. CONCLUSION

The function of a multilayer or an assembly unit is not only defined by putting a number of base materials on a stack. It has to be the strategy to integrate all partners from circuit design to PCB production and assembly. This assumes communication on a high level. Developed requirements must be integrated systematically. Therefore a reliable organisation is needed. Because assembly production is dynamically, information must be handled carefully.

A CAD-layout, a PCB or an assembly can only be done with a reliability directly proportional to the quality of information which is available during routing or producing or assembling the electronic device.

Materials and production processes must be known by all participants.

Professional responsibility decides. Only qualified and continuous education of all people who fabricate electronic devices guarantees a reliable function of highspeed units.